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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Koos et al.

Application No.: 10/690,084

Filed: October 20, 2003

Title: METHOD FOR FABRICATION OF SEMICONDUCTOR INTERCONNECT STRUCTURE WITH REDUCED CAPACITANCE, LEAKAGE CURRENT, AND IMPROVED BREAKDOWN VOLTAGE

Attorney Docket No.: NOVLP068/NVLS-2818

Examiner: Vinh, Lan

Group: 1765

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on September 6, 2006 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Leslie Russell

INFORMATION DISCLOSURE STATEMENT BEFORE FINAL ACTION OR NOTICE OF ALLOWANCE (37 CFR §§ 1.56 AND 1.97(c))

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references listed in the attached PTO Form 1449, a copy of which is attached, may be material to examination of the above-identified patent application. Applicants submit this reference in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make this citation of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that this reference indeed constitutes prior art.

This Information Disclosure Statement is being filed after the mailing date of the first Office Action on the merits, or after three months of the filing date of this application, whichever event occurred last, but it is believed before the mailing date of either: (i) a final action under

§1.113 or (ii) a notice of allowance under §1.311, whichever occurs first.

Accompanying this Information Disclosure Statement is

☐ a statement as specified in 37 CFR 1.97(e); or

☒ the fee set forth in 37 CFR 1.17(p).

If fees are due, enclosed is our Check No. 12341 for $180.00 in payment of the Information Disclosure Statement Fee. If it is determined that any additional fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. NOVLP068).

Respectfully submitted,
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Form 1449 (Modified) **Information Disclosure Statement By Applicant** (Use Several Sheets if Necessary)	Atty Docket No. NOVLP068/NVLS-2818 Applicant: Koos et al. Filing Date October 20, 2003	Application No.: 10/690,084 Group 1765

U.S. Patent and Publication Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A1	4,002,778	1/11/77	Bellis et al.			
	A2	6,692,873	11/8/05	Park			
	A3	5,824,599	10/20/98	Schacham-Diamond, et al.			
	A4	5,695,810	12/9/97	Dubin et al.			
	A5	5,380,560	1/10/945	Kaja et al.			
	A6	6,197,364	3/6/01	Paunovic et al.			
	A7	2002/0084529	07/2002	Dubin et al.			
	A8	2003/0176049	09/2003	Hegde et al.			

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	B1	JP03122266	05/1991	JPO				

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	C1	Sullivan et al, "Electrolessly Deposited Diffusion Barriers For Microelectronics, E. J. IBM J Res Develop Vol 42, No. 4 Sept 1998, 607-620
	C2	Eugene J. O"Sullivan, "Electroless Deposition in Microelectronics: New Trend," Electrochemical Society Proceeding Volume 99-34, 159-171
	C3	T. Itabashi et al., "Electroless Deposited CoWB for Copper Diffusion Barrier Metals," Hitachi Research Laboratory, IEEE, 2002, 285-287
	C4	N. Petrov and Y. Shacham-Diamand, "Electrochemical Study of the Electroless Deposition of Co(W,P) Barrier Layers for Cu Metallization," Electrochemical Soc. Proceedings Vol. 2000-27, 134-148

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	C5	Yosi Shacham-Diamand and Sergey Lopatin, "Integrated Electroless Metallization for ULSI," Elecrochimica Acta, (44 (19999) 3639-3649
	C6	Theoretical Studies on the Electroless Metal Deposition Reaction Mechanism Group, printed from website http://www.appchem.waseda.ac.jp on 7/3/02. Published prior to the filing of this application. 3 Pages
	C7	Wolf, Silicon Processing for the VLSI Era, Lattice Press, Vol. 3, Page 648

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.